Rowhammer.js: Root privileges for web apps?

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December 28, 2015 — 32c3, Hamburg, Germany

Clémentine Maurice
PhD since October
from Rennes, France

Daniel Gruss
PhD student
from Graz, Austria

Both of us started to work independently on cache attacks

Bit flips! — The timeline

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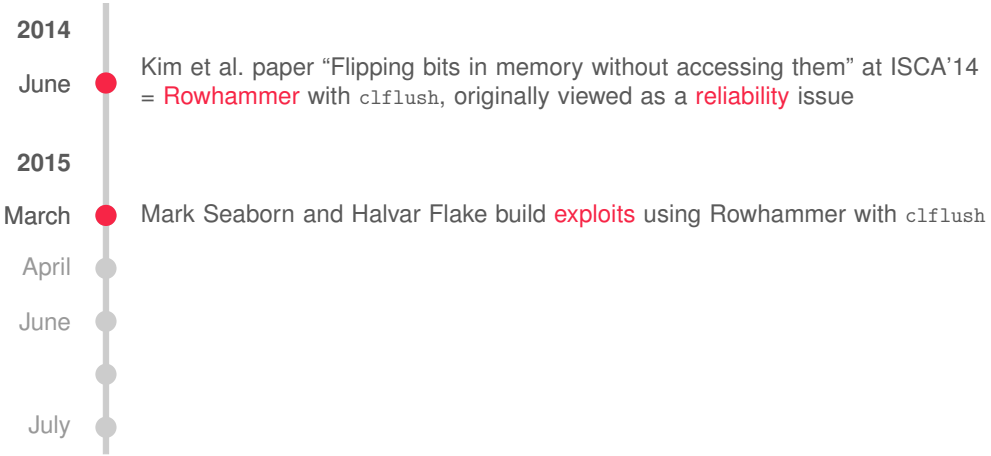

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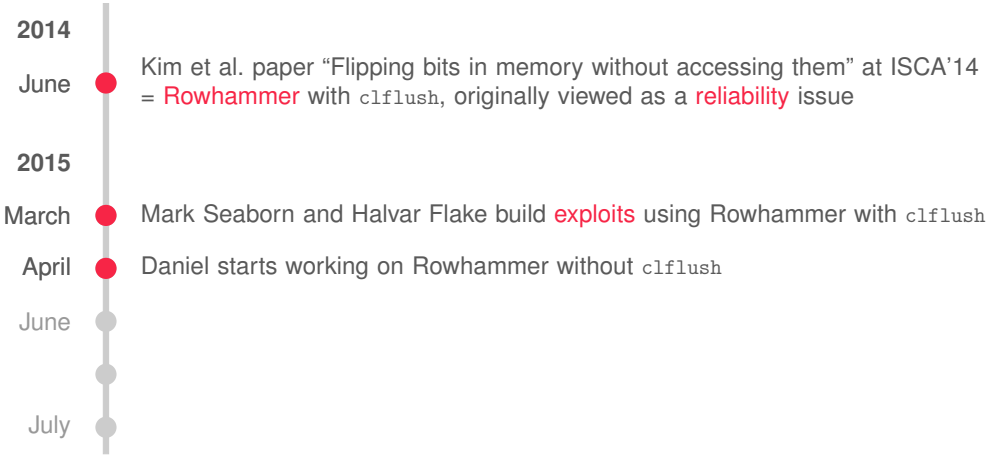

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July — Bit flips in JavaScript!

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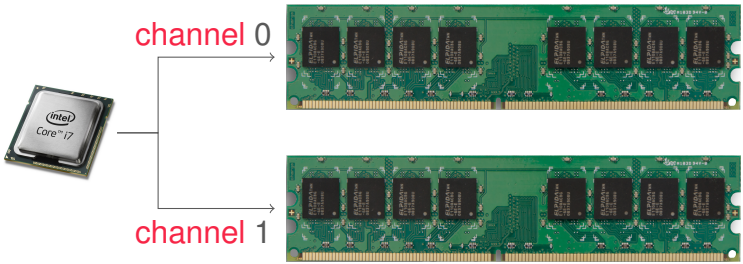

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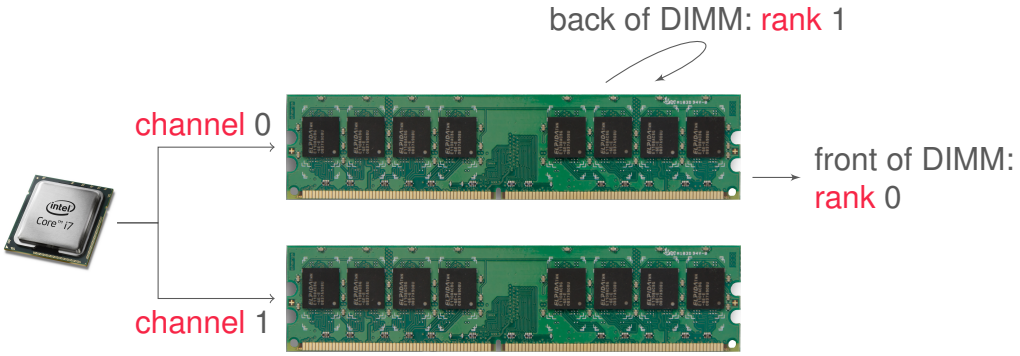

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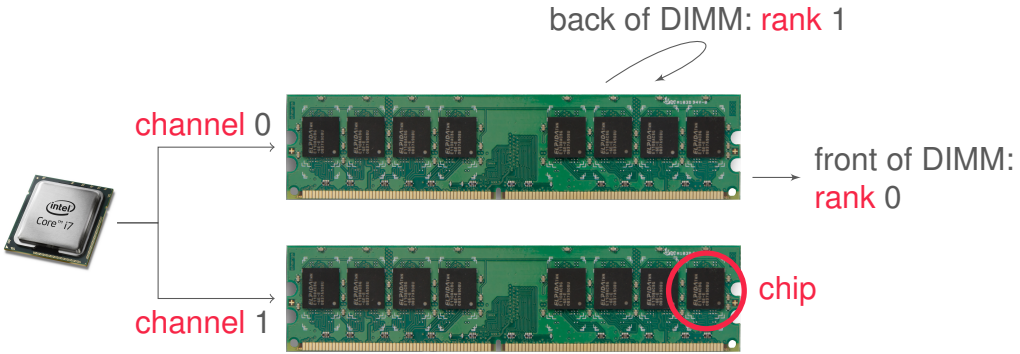

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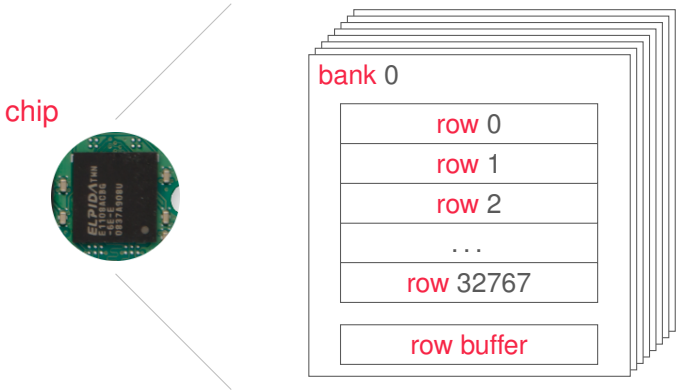

- bits in cells in rows
- access: activate row, copy to row buffer
- cells leak $\rightarrow$ refresh necessary
- cells leak faster upon proximate accesses

Rowhammer

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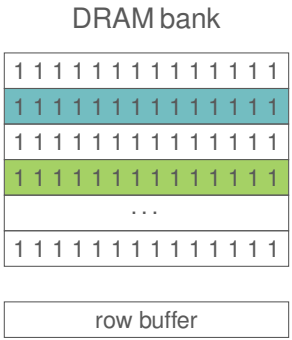

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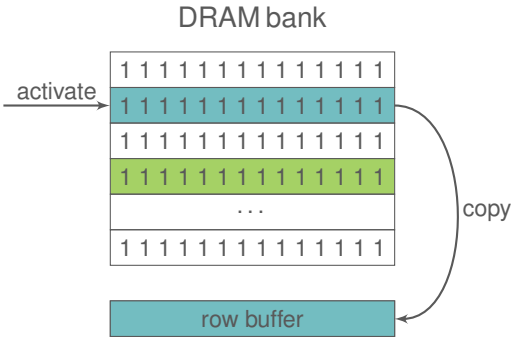

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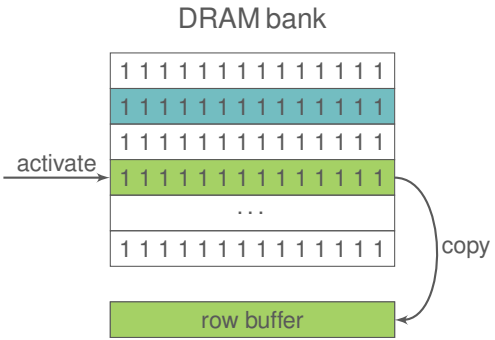

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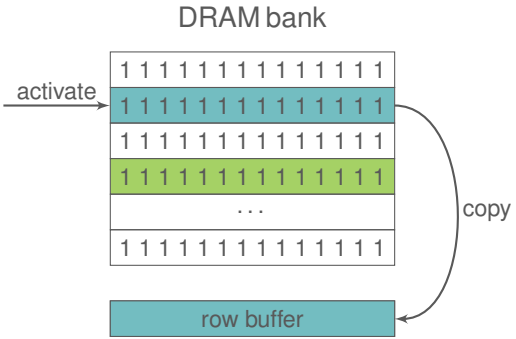

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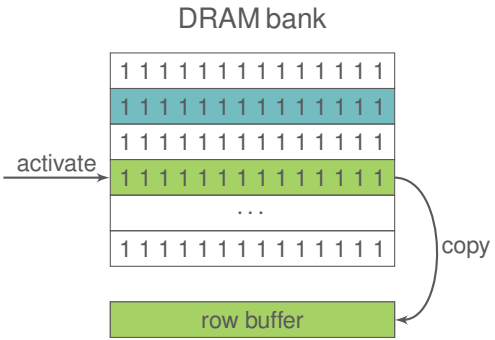

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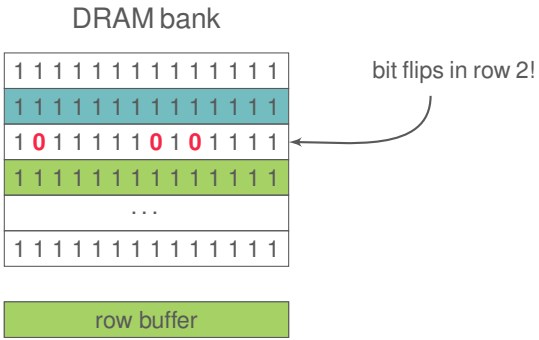
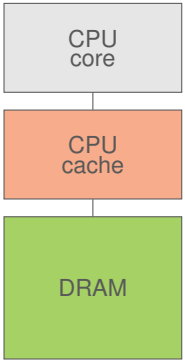


Impact of the CPU cache

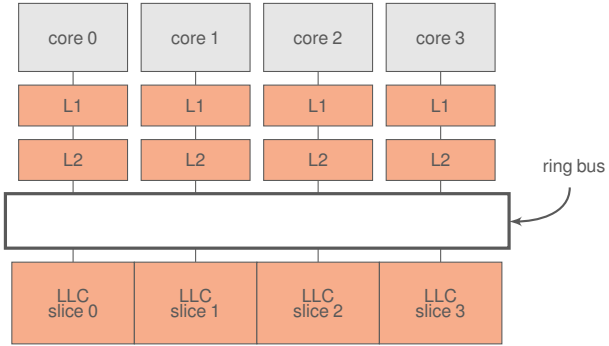


- only non-cached accesses reach DRAM
- original attacks use `clflush` instruction

→ flush line from cache

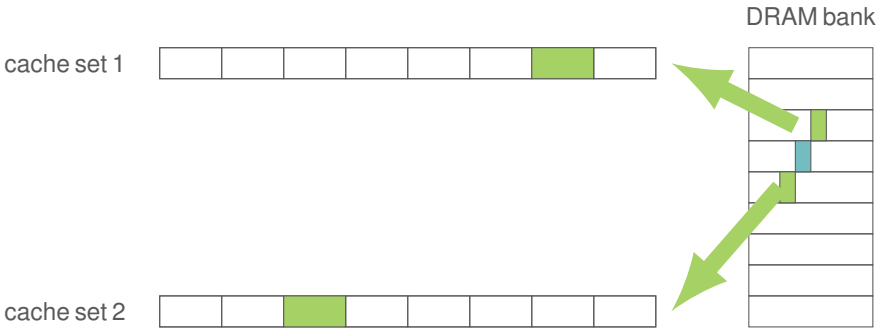
→ next access will be served from DRAM

Cache background



- L1 and L2 are private
- last-level cache:
  - divided in slices
  - shared across cores
  - inclusive

Rowhammer (with `clflush`)



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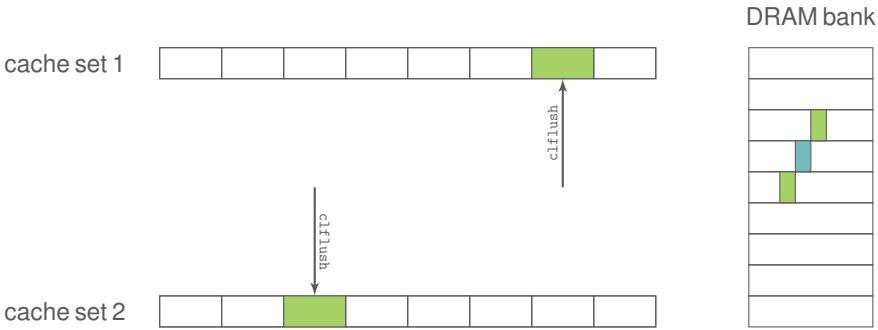

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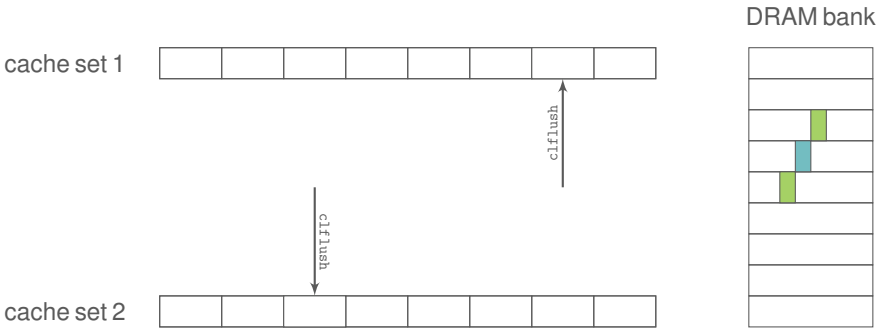

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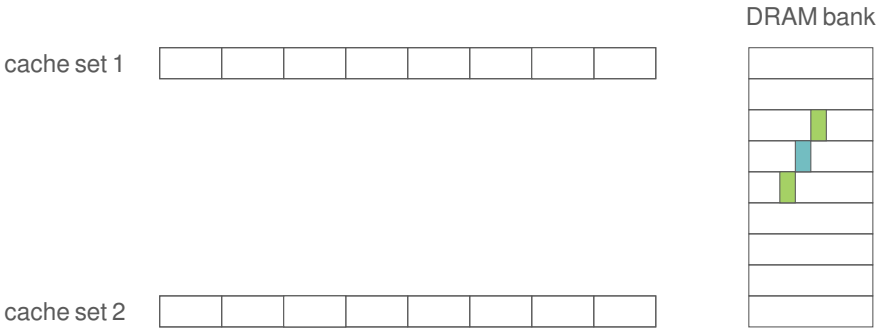

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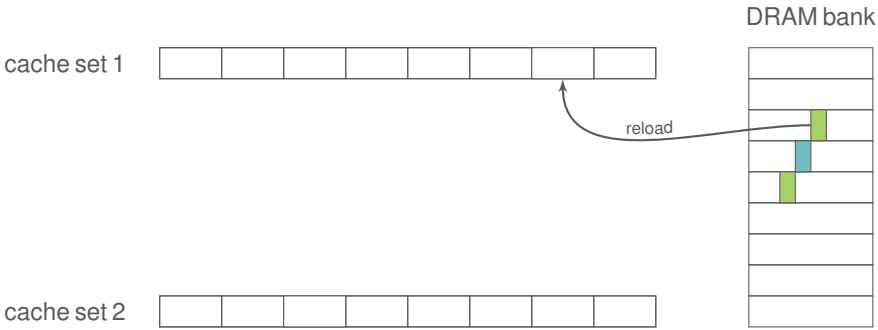

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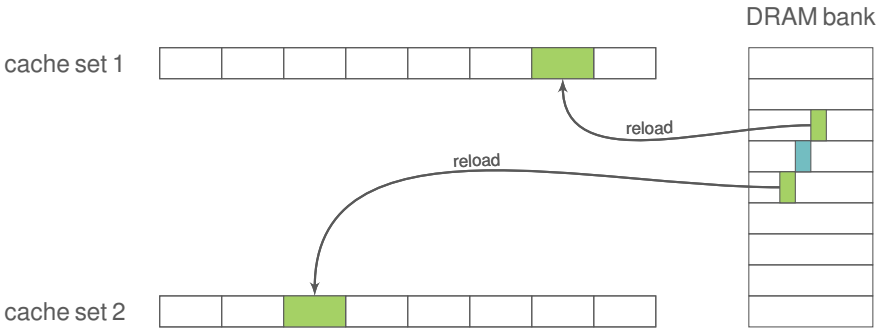

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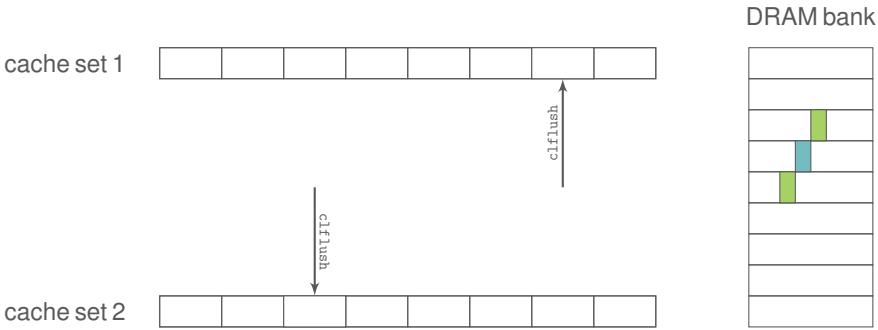

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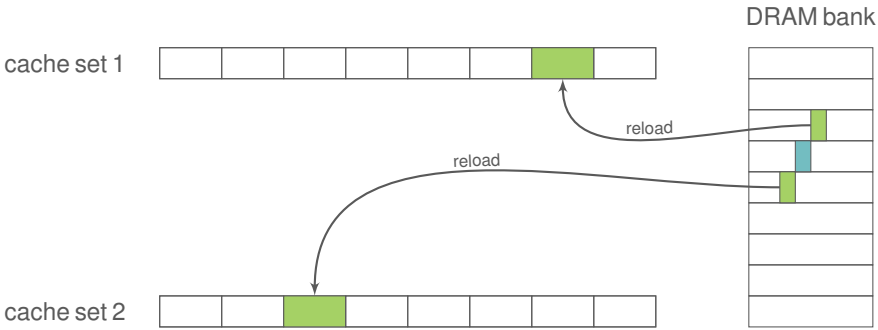

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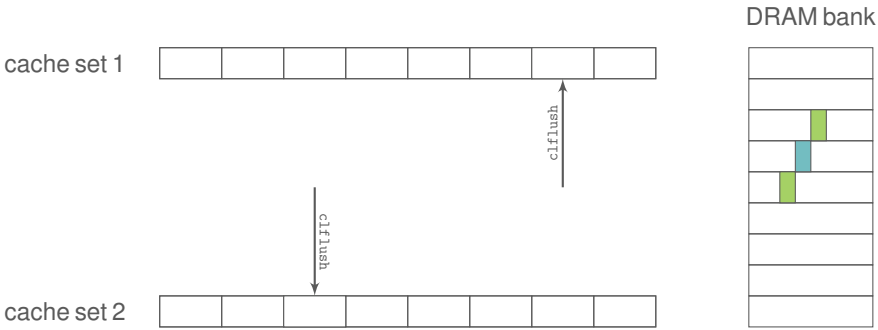

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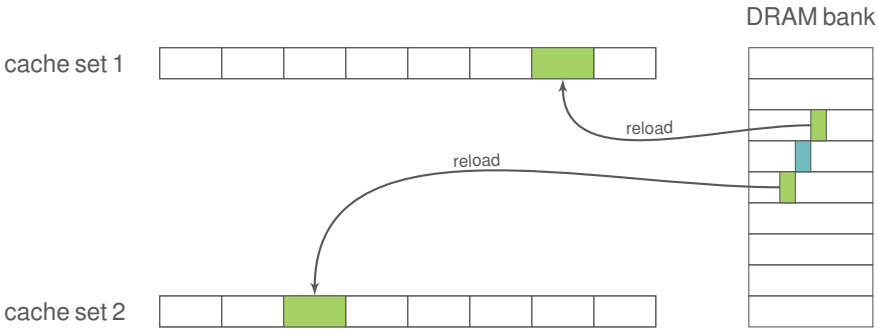

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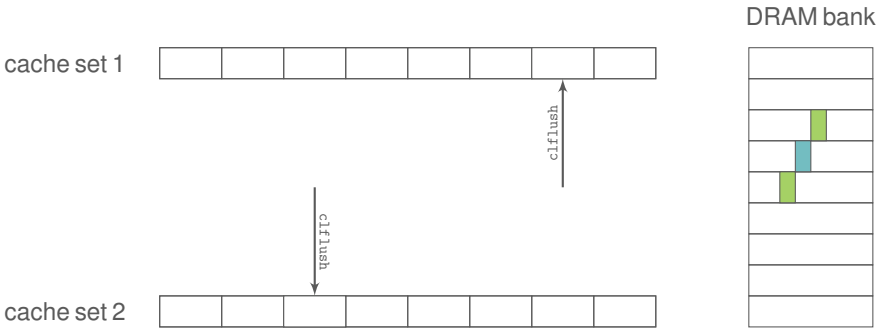

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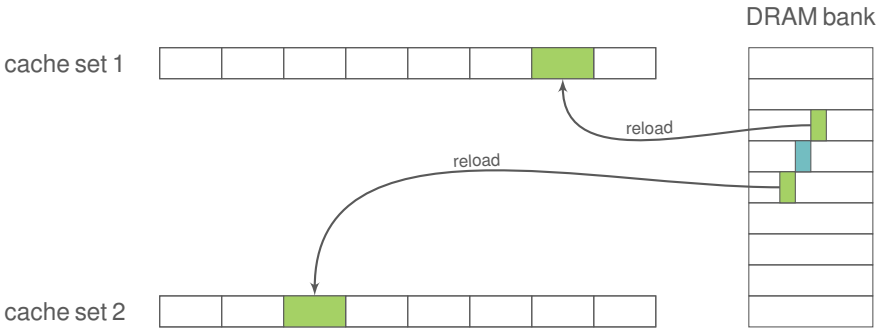

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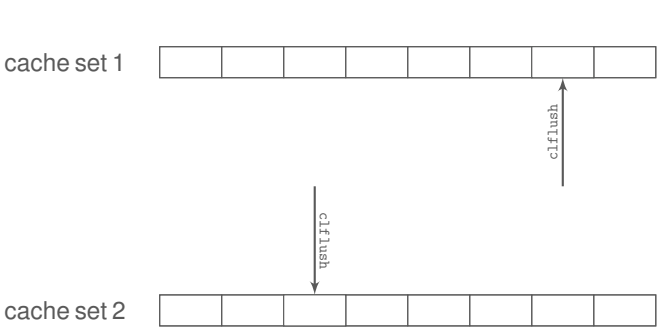

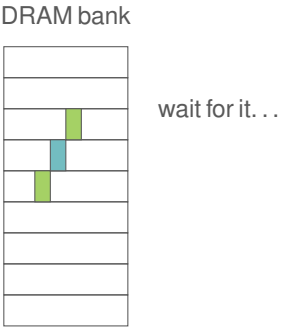

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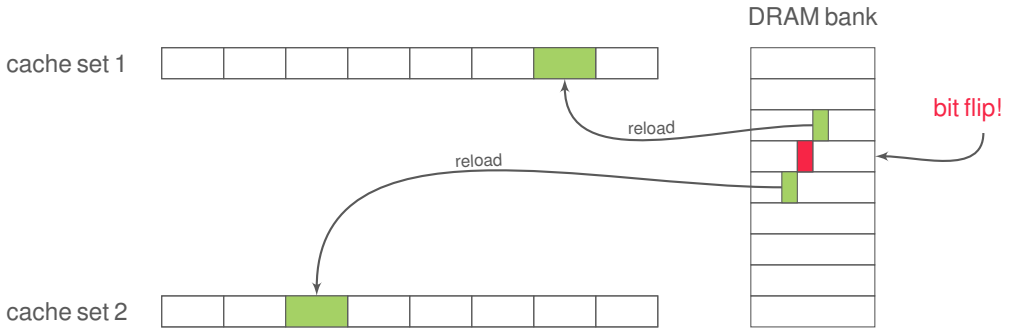

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- automated attacks [Gruss et al., 2015c]
- crypto keys, keylogging, cross VM attacks, ...

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  → no `clflush` in JavaScript
- our approach: use regular memory accesses for eviction
  → techniques from cache attacks!

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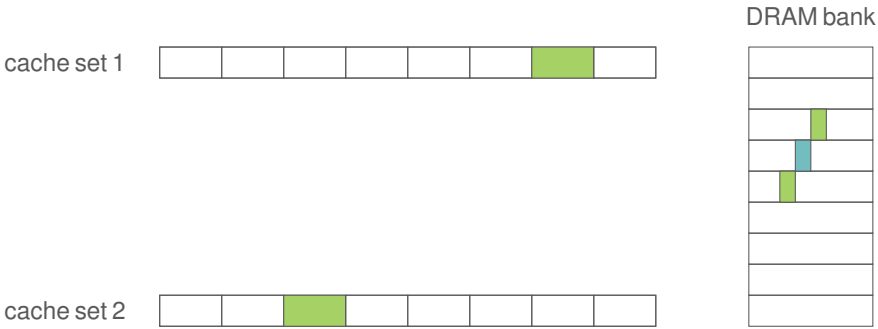

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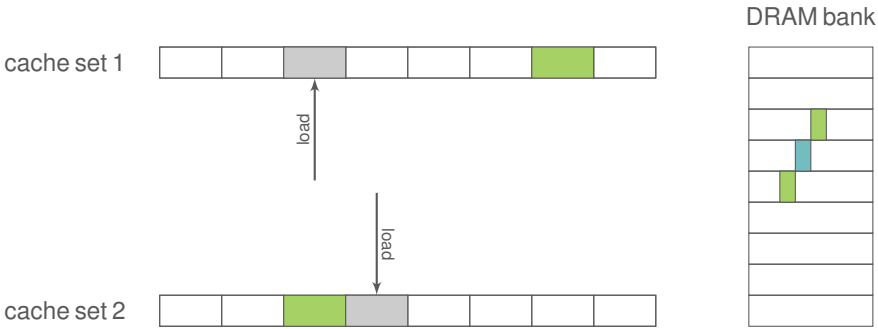

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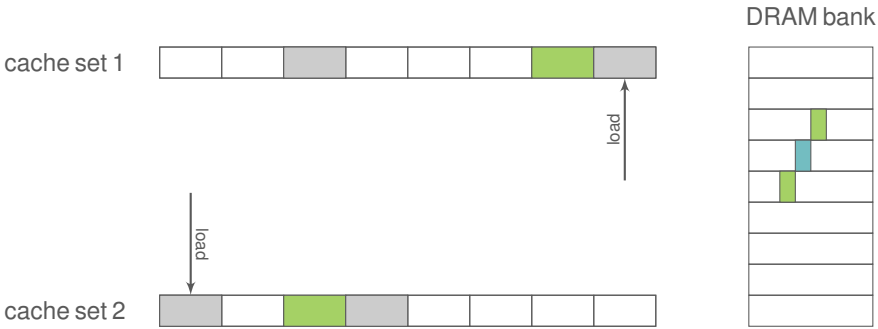

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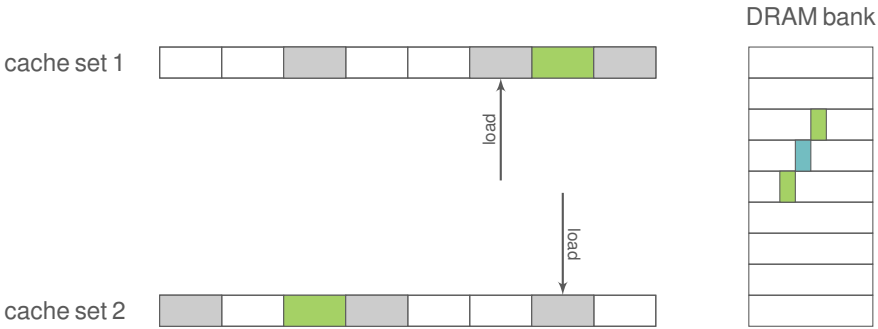

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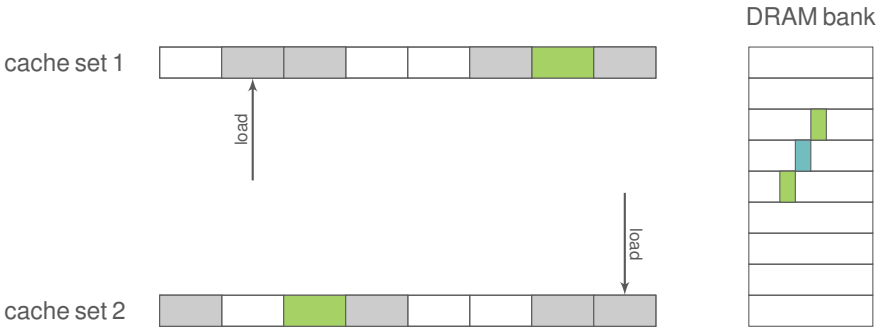

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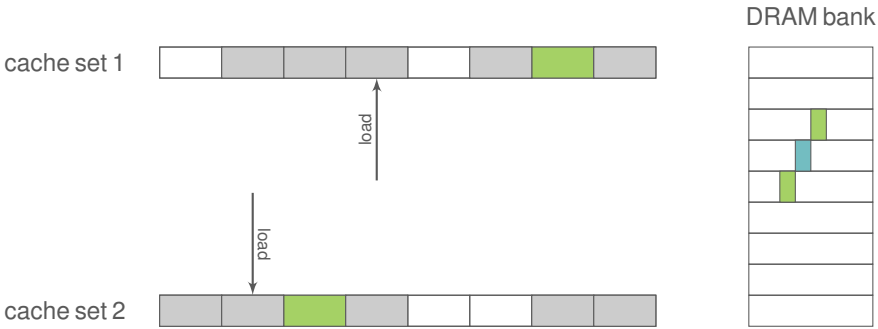

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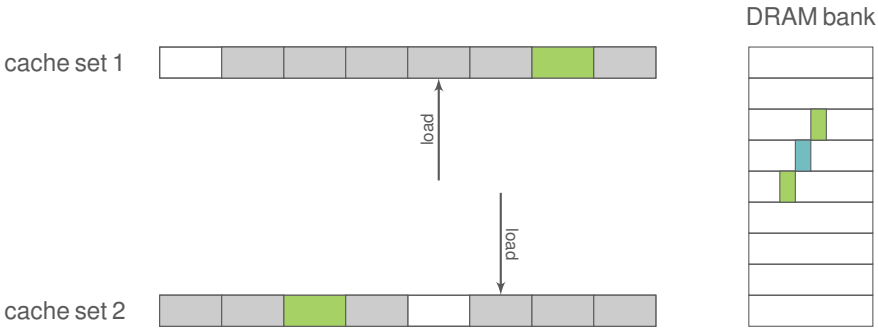

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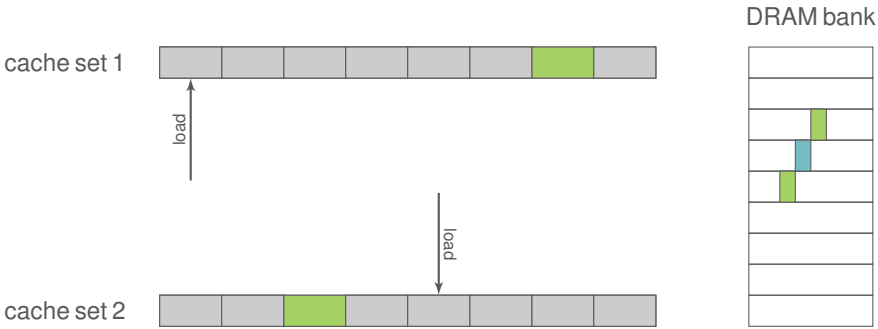

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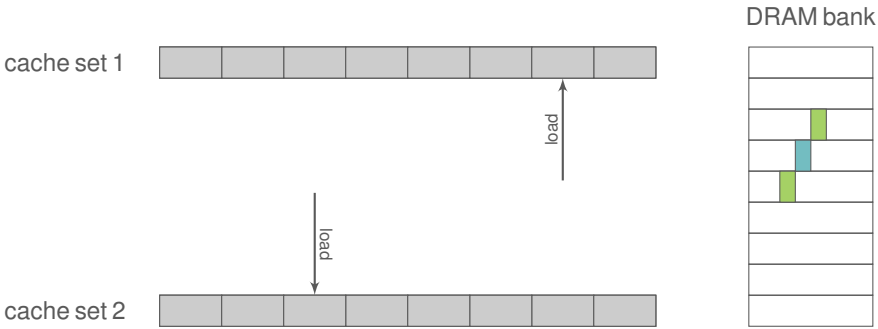

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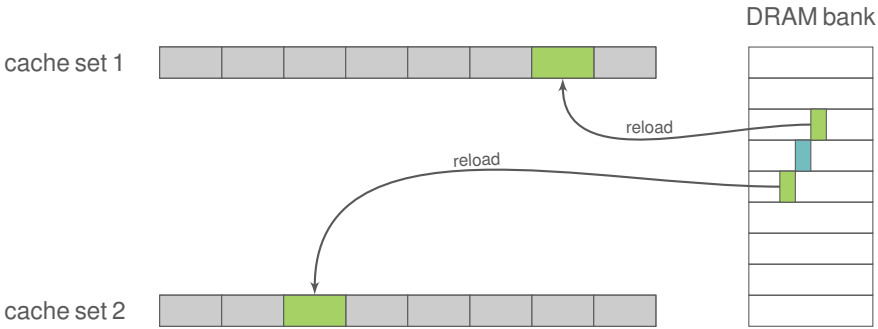

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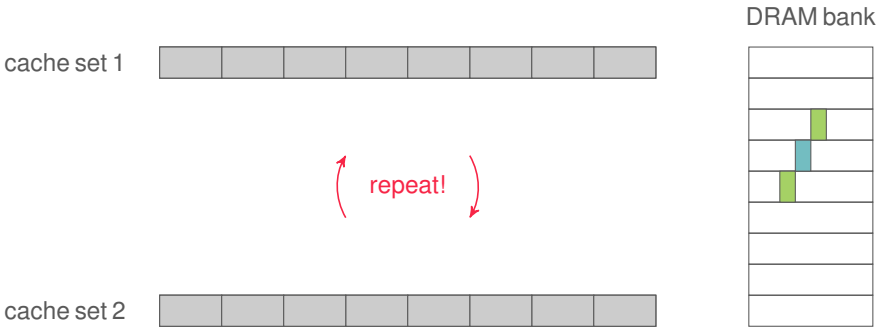

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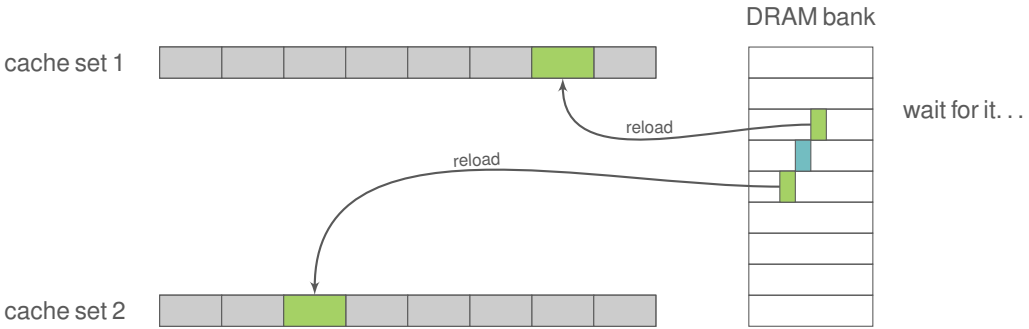

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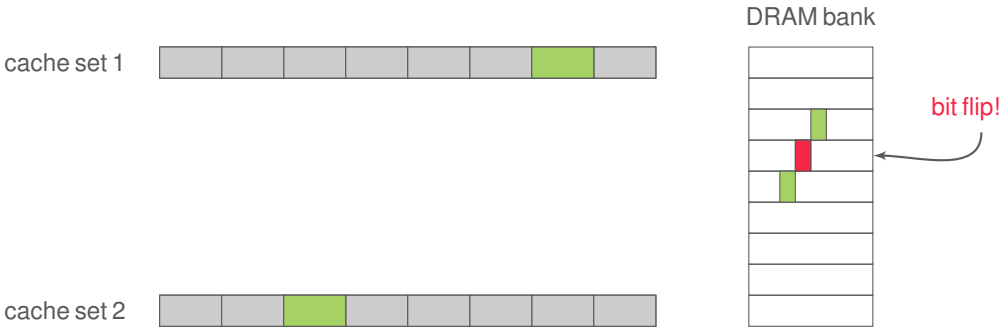

Rowhammer.js: the challenges

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2. Which physical addresses to access?
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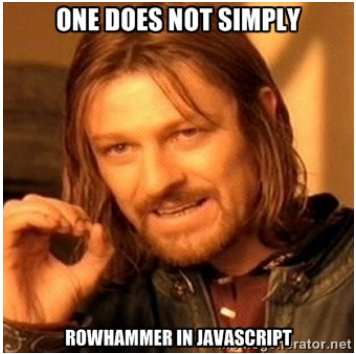

#1.1: Physical addresses and DRAM

- fixed map: physical addresses $\rightarrow$ DRAM cells
- undocumented for Intel
- reverse-engineering by [Seaborn, 2015b] for Sandy Bridge
- and by us [Pessl et al., 2015] for Sandy, Ivy, Haswell, Skylake, ...

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- = last 21 bits (2MB) of virtual address
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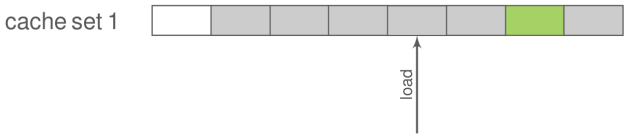
- several DRAM rows per 2MB page
- several congruent addresses per 2MB page
- use timing for cross-page information

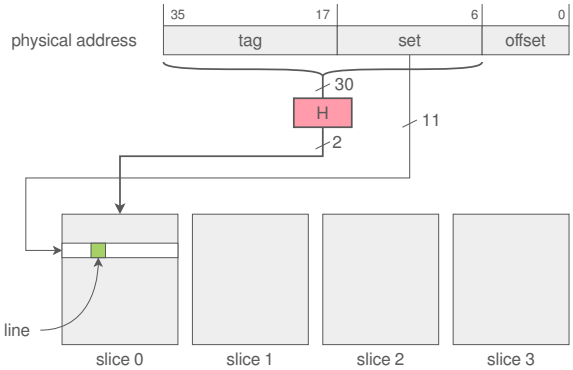
#2.1: Which physical addresses to access?



“LRU eviction”:

- assume that cache uses LRU replacement
- accessing n addresses from the same cache set to evict an n-way set
  [Percival, 2005, Liu et al., 2015, Oren et al., 2015, Maurice et al., 2015b]
- eviction from last level $\rightarrow$ from whole hierarchy (it’s inclusive!)

#2.2: Which addresses map to the same set?



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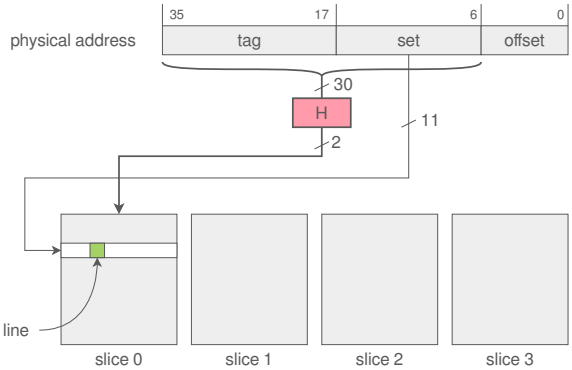

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- hash function basically an XOR of address bits

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- function H that maps slices is undocumented
- reverse-engineered by [Maurice et al., 2015a, Inci et al., 2015, Yarom et al., 2015]
- hash function basically an XOR of address bits

#3.1: Replacement policy on older CPUs

“LRU eviction” memory accesses

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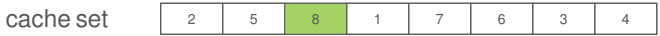

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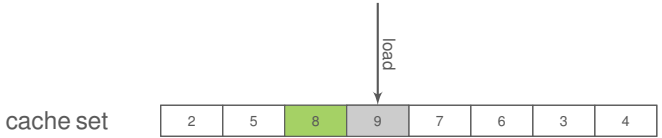

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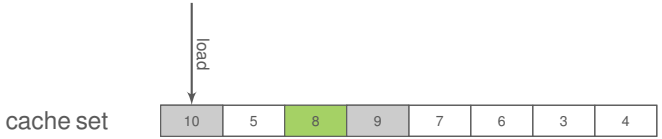

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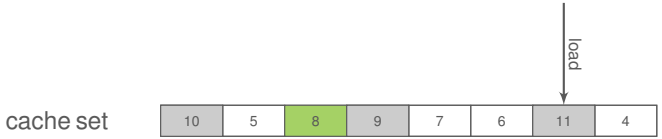

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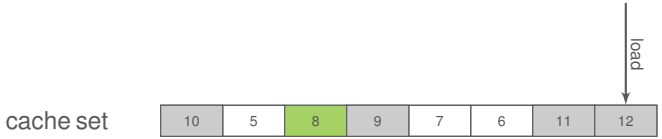

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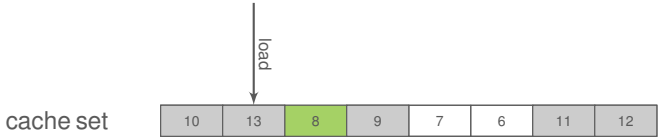

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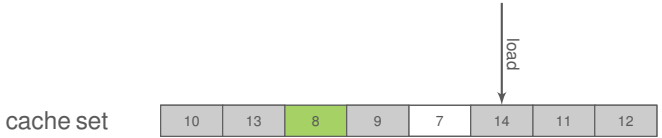

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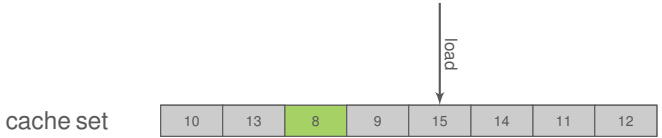

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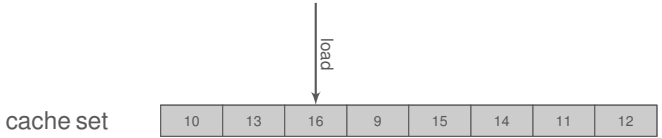

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#3.2: Replacement policy on recent CPUs

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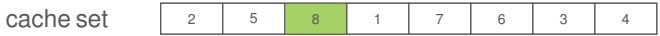

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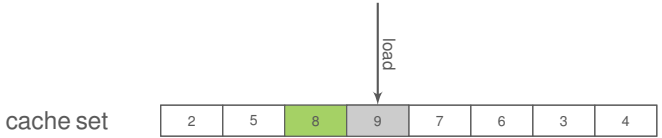

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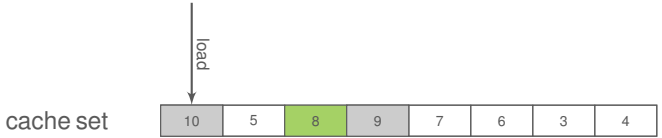

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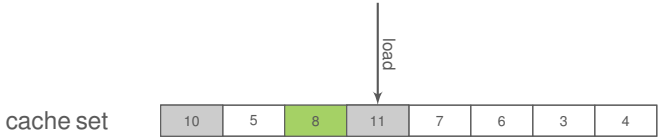

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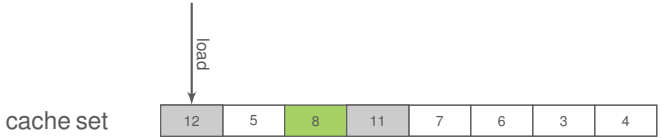

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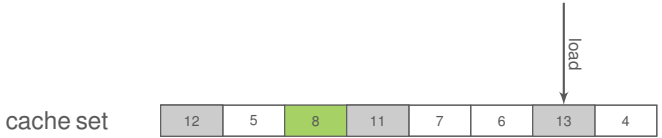

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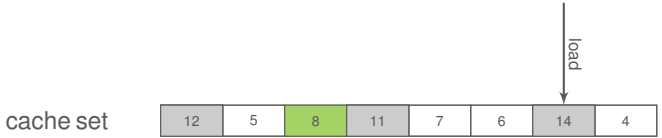

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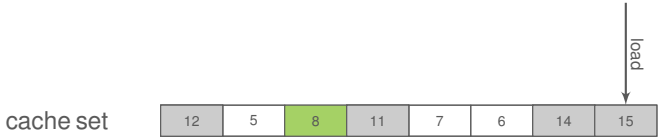

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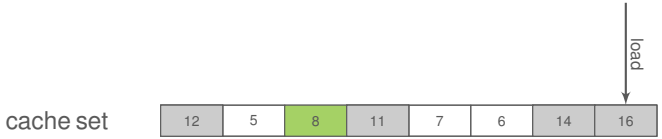

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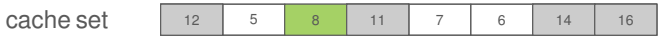

- no LRU replacement
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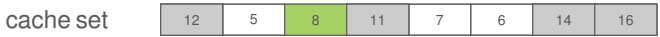

- no LRU replacement
- only 75% success rate on Haswell
- more accesses → higher success rate, but too slow

#3.3: Cache eviction strategy

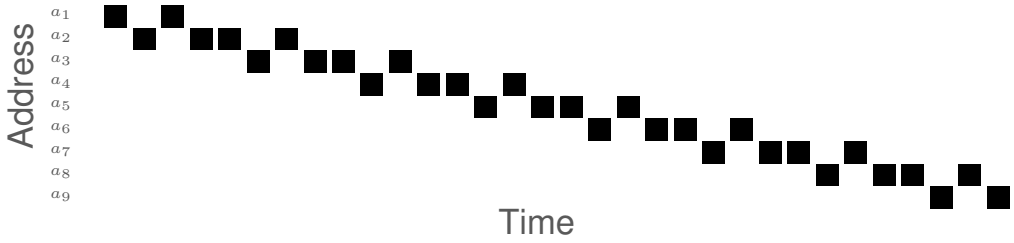

Figure: Fast and effective on Haswell. Eviction rate $>$99.97%.

#4: How to get accurate timing in JavaScript?

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- native code: `rdtsc`
- JavaScript: `window.performance.now()`
- recent patch: time rounded to 5 microseconds
- still works - we measure millions of accesses

Evaluation on Haswell

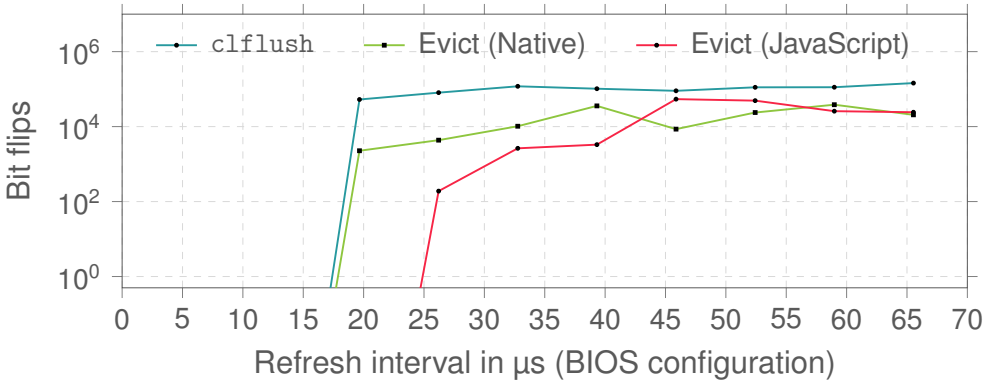

Figure: Number of bit flips within 15 minutes. [Gruss et al., 2015b]

Exploits?

Idea: port root exploit by [Seaborn, 2015a] to JavaScript

- page table spraying
- needs shared memory $\rightarrow$ not available in JavaScript

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- page table spraying
- needs shared memory $\rightarrow$ not available in JavaScript
- zero pages are deduplicated
  - “shared memory” accessible from JavaScript

Physical memory access exploit in native code

1. find exploitable bitflip (address bit)
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Code execution as root

1. search for `/bin/sh` binary pages, ...
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3. wait until root executes shellcode

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- patch OS: life is not perfect – that's ok!
  - idea: we don't care about self-destructive processes
  - → same-privilege physical memory pools

Conclusions

- cache eviction fast enough to replace `clflush`
- independent of programming language and available instructions
- hardware-fault attack induced in JavaScript

$\rightarrow$ remote attacks through websites

Not there yet, but ...

ROOT privileges for web apps!

Rowhammer.js: Root privileges for web apps?

Daniel Gruss (@lavados)[1], Clémentine Maurice (@BloodyTangerine)[2]
[1]IAIK, Graz University of Technology / [2]Technicolor and Eurecom

December 28, 2015 — 32c3, Hamburg, Germany

[Gruss et al., 2015a] Gruss, D., Bidner, D., and Mangard, S. (2015a).

Practical memory deduplication attacks in sandboxed javascript.

In *Proceedings of the 20th European Symposium on Research in Computer Security (ESORICS'15)*.

[Gruss et al., 2015b] Gruss, D., Maurice, C., and Mangard, S. (2015b).

Rowhammer.js: A Remote Software-Induced Fault Attack in JavaScript.

arXiv:1507.06955v1.

[Gruss et al., 2015c] Gruss, D., Spreitzer, R., and Mangard, S. (2015c).

Cache Template Attacks: Automating Attacks on Inclusive Last-Level Caches.

In *USENIX Security Symposium (USENIX Security'15)*.

[Inci et al., 2015] Inci, M. S., Gulmezoglu, B., Irazoqui, G., Eisenbarth, T., and Sunar, B. (2015).

Seriously, get off my cloud! Cross-VM RSA Key Recovery in a Public Cloud.

Cryptology ePrint Archive, Report 2015/898.

[Kim et al., 2014] Kim, Y., Daly, R., Kim, J., Fallin, C., Lee, J. H., Lee, D., Wilkerson, C., Lai, K., and Mutlu, O. (2014).

Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors.

In *ACM/IEEE International Symposium on Computer Architecture (ISCA'14)*.

[Liu et al., 2015] Liu, F., Yarom, Y., Ge, Q., Heiser, G., and Lee, R. B. (2015).

Last-Level Cache Side-Channel Attacks are Practical.

In *IEEE Symposium on Security and Privacy (S&P'15)*.

[Maurice et al., 2015a] Maurice, C., Le Scouarnec, N., Neumann, C., Heen, O., and Francillon, A. (2015a).

Reverse Engineering Intel Last-Level Cache Complex Addressing Using Performance Counters.

In *International Symposium on Research in Attacks, Intrusions and Defenses (RAID)*.

[Maurice et al., 2015b] Maurice, C., Neumann, C., Heen, O., and Francillon, A. (2015b).

C5: Cross-Cores Cache Covert Channel.

In *International Conference on Detection of Intrusions and Malware, and Vulnerability Assessment (DIMVA'15)*.

[Oren et al., 2015] Oren, Y., Kemerlis, V. P., Sethumadhavan, S., and Keromytis, A. D. (2015).

The Spy in the Sandbox: Practical Cache Attacks in JavaScript and their Implications.

In *ACM Conference on Computer and Communications Security (CCS'15)*.

[Percival, 2005] Percival, C. (2005).

Cache Missing for Fun and Profit.

URL: `http://daemonology.net/hyperthreading-considered-harmful/`.

[Pessl et al., 2015] Pessl, P., Gruss, D., Maurice, C., Schwarz, M., and Mangard, S. (2015).

Reverse Engineering Intel DRAM Addressing and Exploitation.

arXiv:1511.08756.

[Seaborn, 2015a] Seaborn, M. (2015a).

Exploiting the DRAM rowhammer bug to gain kernel privileges.

`http://googleprojectzero.blogspot.com/2015/03/exploiting-dram-rowhammer-bug-to-gain.html`.

[Seaborn, 2015b] Seaborn, M. (2015b).

How physical addresses map to rows and banks in DRAM.

http://lackingrhoticity.blogspot.com/2015/05/how-physical-addresses-map-to-rows-and-banks.html.

[Yarom et al., 2015] Yarom, Y., Ge, Q., Liu, F., Lee, R. B., and Heiser, G. (2015).

Mapping the Intel Last-Level Cache.

Cryptology ePrint Archive, Report 2015/905.

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