Milkymist, an open hardware VJ platform

Technical overview

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1 Introduction

The Milkymist™ project [1] develops a standalone device in a small form factor that is capable of rendering MilkDrop-esque visuals effects [12] in real time, with a high level of interaction with many sensors and using live audio and video streams as a base.

Open source components and design tools have been developed or used as much as possible. A system-on-chip implemented in a FPGA has been chosen for meeting this goal at the IP core level.

The flexibility of the FPGA enables advanced users to modify the design, and also permits compact integration of many interfaces (MIDI, OSC, DMX512, analog sensors, video inputs), making Milkymist™ a platform of choice for the mobile VJ.

The design is also highly modular and documented, making the code easy to re-use in other open source system-on-chips.

This paper gives a technical overview of the FPGA-based system-on-chip and its environment.

2 System architecture

The block diagram of the complete system-on-chip is given in Figure 1. The complete system is written in synthesizable Verilog HDL. Its components are detailed below.

2.1 SoC interconnect

The Milkymist system-on-chip uses three different kind of buses :

- WISHBONE [9] as a general purpose bus around the CPU core.
- a custom "CSR" bus [2] used to access configuration and status registers of peripherals. It is simpler than WISHBONE; it does not support variable latency and the address decoding is simplified.
- a custom "FastMemoryLink" (FML) bus [3] which is pipelined and burst-oriented for efficient DRAM access.

By removing the need for logic that is only required to comply with a too general bus specification, the use of these specific buses reduce the hardware design effort and improve resource efficiency.

2.2 Building blocks

2.2.1 Base system

The base system is made up of a Mico32 CPU core [8], on-chip SRAM, off-chip Flash, an UART for printing debug messages, general-purpose I/O ports, timers, and interrupt controller.

The Mico32 core can execute uClinux [11], or be programmed like a microcontroller, without operating system.

There are plans to use AEMB [15] instead of Mico32.

These make up a basic system that is capable of executing software and communicate with the outside world. On top of this system, special peripherals and accelerators are added.

2.2.2 Memory interface

The system-on-chip is equipped with a custom DDR SDRAM controller [4], supporting a FastMemoryLink interface.

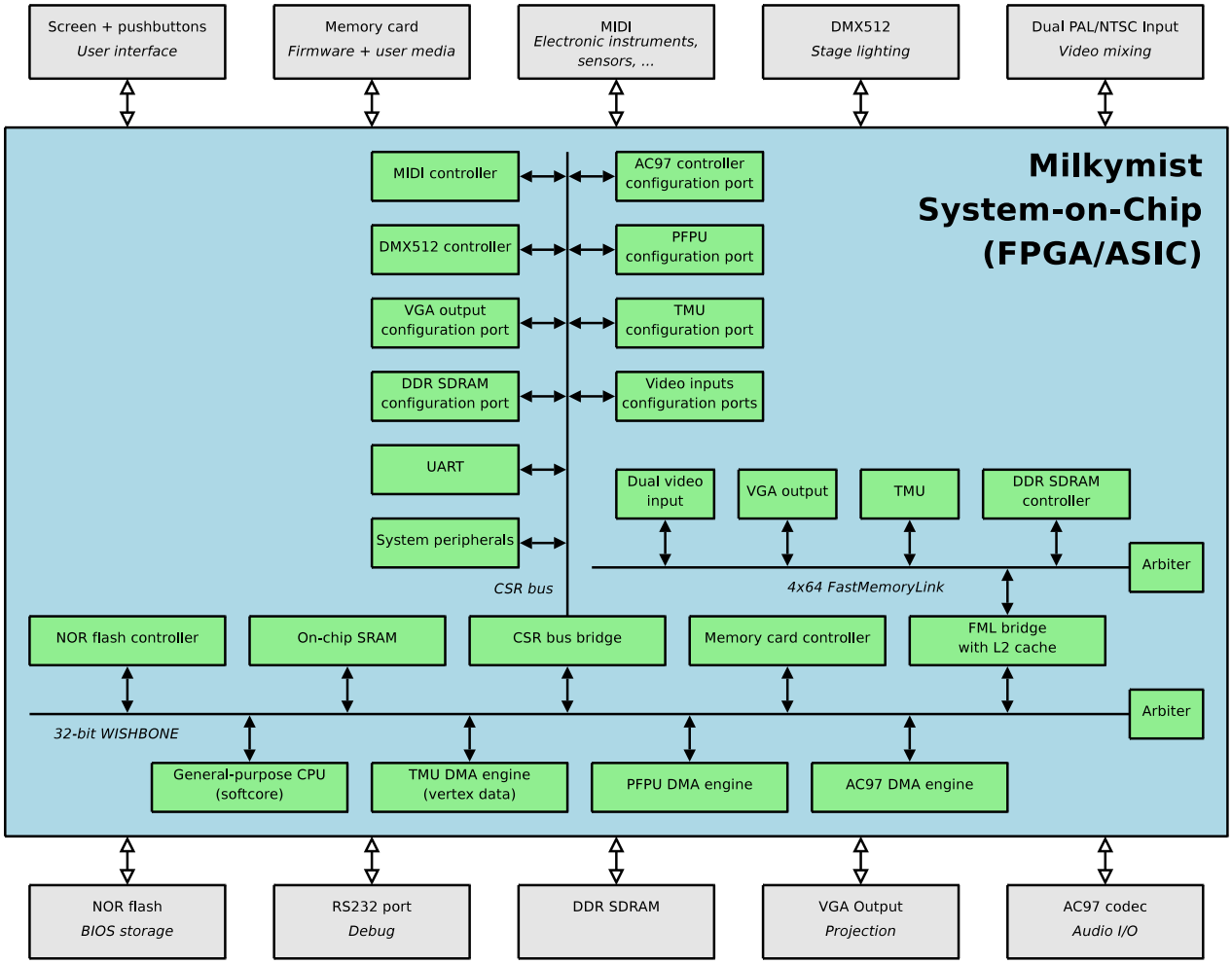

Fig. 1: SoC block diagram

The DDR SDRAM data bus width is 32 bits and is running at 100MHz, delivering a peak (ideal) memory bandwidth of 6.4Gbps.

The memory controller is fully synchronous (the SDRAM clock is the system clock) to avoid clock domain crossing delays and reduce the overall memory latency.

It is a "page mode" controller, which leaves DRAM pages open after an access on the chance that the next access will be on the same page. This has been shown to be fruitful in most cases [13].

Memory latencies are further reduced by the use of pipelined transfers on the FML bus.

2.2.3 VGA output

The system-on-chip directly drives the H/V synchronization pins of the VGA interface and a video DAC that generates the red, green and blue analog signals.

The framebuffer is read from DRAM using the FML interface directly.

To cope with the hard realtime constraint of the video signal generation, the VGA controller contains a FIFO which hides the memory latencies.

The framebuffer uses a simple progressive scan 16bpp RGB565 schema. The controller supports multiple buffering and synchronizes the switching between the framebuffers with the vertical blanking intervals in order to prevent drawing artifacts.

2.2.4 Texture mapping unit (TMU)

The unit maps a texture on a surface defined by a triangle strip.

To implement MilkDrop at a good frame rate, this becomes a very computation and memory intensive process. The implementation is heavily parallel, and is directly connected to the FML bus to acheive memory bandwidth constraints [5] [7].

2.2.5 Programmable floating point unit (PFPU)

The PFPU [6] is a floating point coprocessor, whose primary purpose is generating vertex data when implementing MilkDrop.

It is a pipelined VLIW processor with all the scheduling done by the compiler. Loop structures are not programmable, which limits the use case to evaluating mathematical expressions.

2.2.6 Audio I/O

The audio controller interfaces the system-on-chip to industry-standard and cheap AC97 codecs.

2.2.7 Memory card

The system is equipped with a CompactFlash memory card controller, which is used to store firmware, and user media and data.

2.2.8 Video inputs

Two video inputs compatible with PAL and NTSC are planned to be added to the system.

An external ADC and decoder chip like ADV7181 will be added to simplify the process.

Those video inputs enable the use of the device in live video mixing and transformation applications.

2.2.9 Control peripherals

The following interfaces are planned to be added to the system :

- DMX512 (stage lighting)
- MIDI (electronic instruments)
- Ethernet (OpenSoundControl for electronic instruments)

These make the device suitable for artistic installations and performances.

3 Development system

The system is currently working on a Xilinx ML401 development board equipped with a Virtex-4 XC4VLX25 FPGA. This board integrates most of the peripherals, except DMX512, MIDI and video inputs.

A custom PCB is in development, which will be smaller, have all the interfaces and use a cheaper Spartan-3A FPGA.

On the software side:

- ISE Webpack from Xilinx synthesizes the FPGA bitstream,
- Verilog simulations are run with GPL Cver [14] and Icarus Verilog [16],
- GCC is used to compile the code for the SoC's CPU.

All these tools are either free (as in freedom) or available at no charge.

4 Conclusion

Milkymist features a powerful system-on-chip design, perfectly suited for running embedded applications targeted at video performance artists (VJs). It is also fully open-source (eGPL [10] license), flexible and well documented, allowing its components to be re-used in other system-on-chip designs.

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